Amendment to the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. – 37. (Canceled)

38. (New) A method for processing a semiconductor topography, comprising:

exposing the semiconductor topography to a first low density plasma comprising a first noble gas heavier than helium to etch an anti-reflective layer of the semiconductor topography;

exposing the semiconductor topography to a second low density plasma comprising a second noble gas heavier than helium to etch portions of a nitride layer exposed during the etch of the anti-reflective layer; and

exposing the semiconductor topography to a third low density plasma to etch portions of a polysilicon layer exposed during the etch of the nitride layer.

39. (New) The method of claim 38, wherein the nitride layer comprises a silicon nitride layer, and wherein the method further comprises:

thermally growing the silicon nitride layer upon the polysilicon layer; and

forming the anti-reflective layer upon the silicon nitride layer.

40. (New) The method of claim 38, wherein the steps of exposing the semiconductor topography to the first, second, and third low density plasmas are conducted within the same etch chamber.

41. (New) The method of claim 38, wherein at least two of the first, second and third noble gases differ from one another.

42. (New) The method of claim 38, wherein the step of exposing the semiconductor topography to the first low density plasma comprises introducing the first noble gas into an etch chamber comprising the semiconductor topography at a flow rate between approximately 10 sccm and approximately 100 sccm.

43. (New) A method for processing a semiconductor topography, comprising:

exposing the semiconductor topography to a first low density plasma comprising a first noble gas heavier than helium to etch an anti-reflective layer of the semiconductor topography;

exposing the semiconductor topography to a second low density plasma comprising a second noble gas heavier than helium to etch portions of a first dielectric layer exposed during the etch of the anti-reflective layer; and

exposing the semiconductor topography to a third low density plasma to etch portions of a semiconductor layer exposed during the etch of the first dielectric layer.

44. (New) The method of claim 43, wherein the first dielectric layer comprises silicon oxide and wherein the semiconductor layer comprises a monocrystalline silicon substrate.

45. (New) The method of claim 43, further comprising depositing a second dielectric material upon etched portions of the semiconductor layer to form an isolation region within the semiconductor topography.

46. (New) The method of claim 43, wherein the steps of exposing the semiconductor topography to the first, second, and third low density plasmas are conducted within the same etch chamber.

47. (New) The method of claim 43, wherein at least two of the first, second and third noble gases differ from one another.

48. (New) The method of claim 43, wherein the step of exposing the semiconductor topography to the first low density plasma comprises introducing the first noble gas into an etch chamber comprising the semiconductor topography at a flow rate between approximately 10 sccm and approximately 100 sccm.